

AMENDMENTS TO THE DRAWINGS

To respond to the objection to the drawings, applicants now submit a "REPLACEMENT SHEET" for FIG. 2. The changes proposed by this replacement sheet are the addition of blocks corresponding to the operand polarity register and the operand select register.

As to the objection to the drawings in regard to the ACS engine, it is noted that this element is already present as item 204 in FIG. 2.

Also submitted herewith are "REPLACEMENT SHEETS" for FIGS. 3 and 4. It is proposed to change these drawings by adding "YES" and "NO" labels to the branches from decision blocks 300, 304, 400 and 404.

It is respectfully requested that the Examiner approve these proposed drawing changes.

REMARKS

Claims 1 through 23 are in the application, with Claims 4 and 14 having been amended. Claims 1, 11 and 21 are the independent claims herein. No new matter has been added. Reconsideration and further examination are respectfully requested.

The objection to the drawing has been addressed by the above-noted proposed changes to FIG. 2.

Claim Rejections – 35 USC § 112

It is believed that the rejection of claims 4 and 14 has been overcome by the above-noted amendments to the claims to remove therefrom the language that the Examiner considered to be unclear.

Claim Rejections – 35 USC § 102(e)

Claims 1-3, 8, 11-13, 18 and 21-23 are rejected as being anticipated by Scheuermann U.S. Patent No. 6,577,678 (hereinafter Scheuermann).¹

Before entering a discussion of specific claim language that applicants believe distinguishes the claims from the Scheuermann reference, applicants will first compare the present application with the Scheuermann reference in general terms.

As explained at page 11, lines 8-10 of the specification of this application, the hardware design for a channel decoder may be streamlined, in accordance with the teachings of this application, by using the same add-compare-select (ACS) engine to perform both Viterbi decoding and turbo decoding. In part this is made possible by providing an instruction decoder to cause the ACS engine to perform Viterbi decoding if the instruction decoder receives a first instruction and to perform turbo decoding if the instruction decoder receives a different instruction (see, e.g., page 11, lines 14-20 of the specification).

¹ In view of the ensuing discussion of the Scheuermann reference relative to claim 1, it is not believed that the pending rejection under § 103(a) requires discussion.

By contrast, although the Scheuermann reference does refer to Viterbi decoding, the reference contains no disclosure whatsoever concerning turbo decoding. From this it follows that the reference is not concerned with using the same ACS engine for both Viterbi and turbo decoding, and that the disclosure of the reference is quite different from the subject matter of this application.

Turning now to the specific language of the claims, claim 1 is directed to an “apparatus” which includes “an instruction decoder” and “at least one control register coupled to the instruction decoder”. The apparatus of claim 1 also includes “an add-compare-select (ACS) engine coupled to the at least one control register”. Claim 1 further specifies that “the instruction decoder is operative to control the ACS engine to perform Viterbi decoding in response to the instruction decoder receiving a first instruction, and the instruction decoder is further operative to control the ACS engine to perform turbo decoding in response to the instruction decoder receiving a second instruction”.

Applicants, by their undersigned representative, have carefully studied the Scheuermann reference and have not found any discussion or mention therein of turbo decoding. The portion of the reference cited by the Examiner as showing an instruction decoder (column 3, lines 18 and 19) merely refers to a reduced instruction set (RISC) processor. The portion of the reference cited by the Examiner as allegedly describing operation of the instruction decoder (column 1, lines 66 and 67) refers to a Viterbi decoder element, but does not in any way mention or refer to turbo decoding. No other portion of the reference makes up for the deficiencies of these cited portions. It is therefore submitted that there is no support in the reference for the Examiner’s implied assertion that the reference discloses an instruction decoder operative to control an ACS engine to perform turbo decoding. To reiterate a main point of applicants’ argument, the Scheuermann reference is completely silent as to turbo decoding. If after considering these remarks, the Examiner is still of the opinion that the rejection of claim 1 is well-founded, the Examiner is respectfully challenged to indicate where in the Scheuermann reference turbo decoding is discussed.

Applicants respectfully request that the Examiner reconsider and withdraw the pending rejection of claim 1.

Claims 2-10 are dependent on claim 1 and are submitted as patentable on the same basis as claim 1.

The next independent claim, which is claim 11, includes all of the limitations of claim 1, as well as other limitations. Claim 11 is submitted as patentable on the same basis as claim 1. Claims 12-20 are dependent on claim 11 and are also patentable on the same basis.

The only other pending independent claim is claim 21.

Among other limitations, claim 21 recites operating a forward error correction decoder to perform turbo decoding if an instruction decoder receives a certain instruction. Since Scheuermann, as noted above, contains no disclosure whatever concerning turbo decoding, it follows that claim 21, like claims 1 and 11, cannot be anticipated by the reference. Claims 22 and 23 are dependent on claim 21 and are patentable on the same basis.

CONCLUSION

Accordingly, Applicants respectfully request allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-3460.

Respectfully submitted,

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Date



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